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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/342,235	06/29/1999	YASUHIKO TAKEMURA	0756-1980ELE	6257

7590 03/27/2002

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EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/342,235	TAKEMURA, YASUHIKO
	Examiner	Art Unit
	A. Sefer	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-11* is/are allowed.

6)☒ Claim(s) *1-5 and 12-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
4) ☐ Interview Summary (PTO-413) Paper No(s)
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other

DETAILED ACTION

Response to Amendment

1. The amendment filed on January 1, 2002 has been entered and new claims 13-23 have been added.

Specification

2. The disclosure is objected to because of the following informalities: Line 13 of claim 12 recites "a first insulating film comprising ... formed on the blocking film" and line 18 recites "a first insulating film formed over said substrate" It is not clear whether applicant is referring to the same insulating film or plurality of insulating films. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tskjikawa et al. US Patent No. 5,051,570 in view Hamada et al. (EP 0 414 478 A1).

Tskjikawa et al disclose (see figs. 4 and 9, col. 6, lines 1-7 and lines 30-33 and

col. 12, lines 30-40) a semiconductor device comprising a substrate or glass substrate 128 (as in claim 12) having an insulating surface; a blocking film 121 comprising silicon nitride (as in claim 12); at least first and second semiconductor islands 114, 115 comprising polysilicon (as in claims 5 and 12) formed over said substrate wherein each of the semiconductor islands has a channel region and a pair of impurity regions (unnumbered); an insulating film (see col. 10, lines 49-52) or 200 nm thick insulating film (as in claim 2) formed over said substrate, said insulating film including at least first and second gate insulating films 134, 135 formed over said first and said second semiconductor islands, respectively; at least first and second gate electrodes 112, 113 comprising doped silicon and refractory metal (as in claim 3) formed over said first and second semiconductor islands with said first and second gate insulating films interposed therebetween; a wiring 118 formed on an insulating film wherein said wiring is connected to said one of the impurity regions through a hole (unnumbered) opened in the insulating film; an interlayer insulating film 123 formed over the first and second semiconductor islands, the first and second gate electrodes and wiring; and a pixel electrode 124 formed over said interlayer insulating film electrically connected to one of the pair of the impurity regions of the second semiconductor island.

Hamada et al disclose in fig. 1 a wiring connecting a drain of TFT1 with the gate of TFT2.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to use a wiring connecting an impurity regions of one TFT with a gate electrode of another TFT, since that would enable one transistor to drive another

transistor such that the data signal turns the other transistor ON thereby avoiding the formation of an extra scanning line. It would have been obvious design choice to form a wiring on an insulating film and form a connection through a hole formed thereon as recited in the claim, since that would eliminate the formation of an additional insulating film.

As to claim 4, it would have an obvious design choice to make a pixel electrode using the same compound or ITO as that of a lower electrode 119, since that would save material and processing time.

5. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. US 5,590,555 in view of Hamada et al. (EP 0 414 478 A1).

Yamazaki et al disclose (see fig. 8 and col. 9, lines 5-10 and line 54-63) a semiconductor device comprising a substrate 11 having an insulating surface; at least first and second semiconductor islands comprising polysilicon (as in claim 5) formed over said substrate wherein each of the semiconductor islands has a channel region 28, 28' and a pair of impurity regions 34, 34'; an insulating film 35 or 200 nm thick insulating film (as in claim 2) formed over said substrate, said insulating film including at least first and second gate insulating films formed over said first and said second semiconductor islands, respectively; at least first and second gate electrodes 40, 40' comprising doped silicon and refractory metal (as in claim 3) formed over said first and second semiconductor islands with said first and second gate insulating films interposed therebetween; a wiring 36, 36' formed on said insulating film wherein said wiring is connected to said one of the impurity regions through a hole (unnumbered) opened in

said insulating film; an interlayer insulating film 37 formed over the first and second semiconductor islands, the first and second gate electrodes and wiring; and a pixel electrode comprising ITO (as in claim 4) formed over said interlayer insulating film electrically connected to one of the pair of the impurity regions of the second semiconductor island.

Hamada et al disclose in fig. 1 a wiring connecting a drain of TFT1 with the gate of TFT2.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to use a wiring connecting an impurity regions of one TFT with a gate electrode of another TFT, since that would enable one transistor to drive another transistor such that the data signal turns the other transistor ON thereby avoiding the formation of an extra scanning line.

6. Claims 13-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. US 5,590,555 in view of Hamada et al. (EP 0 414 478 A1).

Yamazaki et al disclose (see fig. 8 and col. 10, lines 36-40) a semiconductor device comprising a substrate 11 having an insulating surface; at least first and second semiconductor islands comprising polysilicon (as in claims 14, 17 and 21) formed over said substrate wherein each of the semiconductor islands has a channel region 28, 28' and a pair of impurity regions 34, 34'; a first and a second gate insulating film formed over said semiconductor island, respectively; at least first and second gate electrodes 40, 40' formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween; an interlayer insulating

film 37 formed over a wiring (as in claims 16 and 19); a smoothing film 39 formed over a wiring (as in claims 20 and 23); a pixel electrode formed over said interlayer insulating film (as in claim 16) or a pixel electrode formed over said smoothing film (as in claim 20) and electrically connected to one of the pair of the impurity regions of the second semiconductor island; wherein the first semiconductor island is a part of an NTFT and the second semiconductor island is a part of a PTFT.

Hamada et al disclose in fig. 1 a wiring connecting a drain of TFT1 with the gate of TFT2.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to use a wiring connecting an impurity regions of one TFT with a gate electrode of another TFT, since that would enable one transistor to drive another transistor such that the data signal turns the other transistor ON thereby avoiding the formation of an extra scanning line.

As to claims 15, 18 and 22, Yamazaki et al disclose a data line electrically connected to one impurity region of an NTFT.

Allowable Subject Matter

7. Claims 6-11 are allowed.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Takasu US reference 5,326,991 discloses a device including a pair of semiconductor islands.

b. Fonash et al US reference 5,275,851 disclose a TFT including source and drain contacting an impurity region through a hole formed on an insulating layer.

c. Unagami et al. US reference 4,528,480 disclose a transistor for driving an EL element.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (703) 308-6601.

ANS
March 24, 2002